Hall Ticket Number:

Code No. : 22615

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) II-Semester Main Examinations, June-2018

(Embedded Systems & VLSI Design)

VLSI Physical Design

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Compare ASIC and FPGA.
2. Explain the structure of capacitor in IC.
3. What is multi finger FET?
4. What are matched components in VLSI?
5. Define lambda based design rules.
6. List the symbols used in stick encoding.
7. Explain the main idea of cell based design.
8. Draw the Logic diagram of 2×1 multiplexer using Transmission gates.
9. What are model parameters?
10. Describe the purpose of parasitic extraction in VLSI layouts.

Part-B (5 × 8 = 40 Marks)

11. a) Explain the steps in NMOS fabrication process. [5]
    b) What are various general VLSI System components? [3]
12. a) What are the components of coupling capacitances and discuss the effects of capacitive coupling between the inter connects. [5]
    b) Explain about common centroid techniques. [3]
13. a) Draw the schematic and Layout to implement $Y = \overline{A.(B+C)}$. [5]
    b) Draw the stick diagram of CMOS BUFFER. [3]
14. a) Explain about Floor planning in VLSI design. [5]
    b) Explain about Weinberger image array. [3]
15. a) Explain about silicon compilers. [5]
    b) Distinguish between Full custom and Semi custom types of VLSI designs. What is design rule checker? [3]
16. a) Explain about clock distribution. [5]
    b) Classify different types of integrated capacitors. [3]
17. Answer any ***two*** of the following:
    a) Explain various fabrication errors that might occur during fabrication of MOS devices. [4]
    b) Different types of design rules. [4]
    c) Standard cell library/Technology library. [4]